**Claim Amendments**

1. (Currently Amended) A method comprising:

using a ~~logic design element~~ first-in-first out (FIFO) memory in a logic design;

performing a simulation of the logic design that includes simulating the ~~logic design element~~ FIFO memory; and

having the ~~logic design element~~ FIFO memory automatically collect and store instrumentation data during the simulation, ~~wherein the instrumentation data represents usage and performance related statistics that relate to the logic design element~~ wherein the instrumentation data collected by the FIFO memory comprises a degree of fullness of the FIFO memory.

2. (Currently Amended) The method of claim 1 further comprising displaying the instrumentation data relating to the ~~logic design element~~ FIFO memory.

3. (Currently Amended) The method of claim 2 further comprising receiving a query to display the instrumentation data relating to the ~~logic design element~~ FIFO memory, wherein displaying the instrumentation data includes displaying the instrumentation data relating to the ~~logic design element~~ FIFO memory in response to the query.

4. (Original) The method of claim 2 wherein displaying the instrumentation data includes displaying the instrumentation data after performing the simulation.

5. (Original) The method of claim 2 wherein displaying the instrumentation data includes displaying the instrumentation data while performing the simulation.

6. (Currently Amended) The method of claim 2 wherein:

performing the simulation includes performing a partial simulation,

having the ~~logic design element~~ FIFO element automatically collect the instrumentation data includes having the ~~logic design element~~ FIFO memory automatically collect the instrumentation data during the partial simulation, and

displaying the instrumentation data includes displaying the instrumentation data after performing the partial simulation.

7. (Canceled).

8. (Currently Amended) The method of claim ~~7~~ 1 wherein having the FIFO memory automatically collect the instrumentation data includes having the FIFO memory record usage of the FIFO memory during the simulation.

9. (Currently Amended) The method of claim ~~7~~ 1 further comprising:

receiving a query to display the ~~instrumentation data relating to~~ degree of fullness of the FIFO memory, and

displaying the ~~instrumentation data relating to~~ degree of fullness of the FIFO memory in response to the query.

10-12. (Canceled).

13. (Previously Presented) A machine-accessible medium, which when accessed results in a machine performing operations comprising:

using a ~~logic design element~~ tri-state bus in a logic design;

performing a simulation of the logic design that includes simulating the ~~logic design element~~ tri-state bus;

having the ~~logic design element~~ tri-state bus automatically collect instrumentation data during the simulation, ~~wherein the instrumentation data represents usage and performance related statistics that relate to the logic design element~~ wherein the instrumentation data collected by the tri-state bus comprises a number of occurrences of bus error conditions experienced by the tri-state bus; and

displaying the instrumentation data relating to the ~~logic design element~~ tri-state bus.

14. (Canceled).

15. (Currently Amended) The machine-accessible medium of claim 13 further comprising receiving a query to display the instrumentation data relating to the ~~logic design element~~ tri-state bus, wherein displaying the instrumentation data includes displaying the instrumentation data relating to the ~~logic design element~~ tri-state bus in response to the query.

16. (Previously Presented) The machine-accessible medium of claim 13 wherein displaying the instrumentation data includes displaying the instrumentation data after performing the simulation.

17. (Previously Presented) The machine-accessible medium of claim 13 wherein displaying the instrumentation data includes displaying the instrumentation data while performing the simulation.

18. (Currently Amended) The machine-accessible medium of claim 13 wherein:

performing the simulation includes performing a partial simulation,

having the ~~logic design element~~ tri-state bus automatically collect the instrumentation data includes having the ~~logic design element~~ tri-state bus automatically collect the instrumentation data during the partial simulation, and

displaying the instrumentation data includes displaying the instrumentation data after performing the partial simulation.

19-22. (Canceled).

23. (Currently Amended) The machine-accessible medium of claim ~~22~~ 13 wherein having the tri-state bus automatically collect the instrumentation data includes having the tri-state bus automatically collect usage of the tri-state bus during the simulation.

24. (Currently Amended) The machine-accessible medium of claim ~~22~~ 13 further comprising:

receiving a query to display the ~~instrumentation data relating to the tri-state bus~~ the number of occurrences of bus error conditions experienced by the tri-state bus, and

displaying the ~~instrumentation data relating to the tri-state bus~~ the number of occurrences of bus error conditions experienced by the tri-state bus in response to the query.

25. (Currently Amended) An apparatus comprising:

a simulation module that is structured and arranged to perform a simulation of a logic design that includes a ~~logic design element~~ tri-state bus;

a collection module that is integrated with the ~~logic design element~~ tri-state bus and that is structured and arranged to automatically collect and store instrumentation data, ~~which represents usage and performance related statistics relating to the logic design element during the simulation~~ wherein the instrumentation data collected by the tri-state bus comprises a number of occurrences of bus error conditions experienced by the tri-state bus; and

a processor to execute modules of the apparatus.

26. (Currently Amended) The apparatus of claim 25 further comprising a display module that is structured and arranged to display the instrumentation data relating to the ~~logic design element~~ tri-state bus.

27. (Currently Amended) The apparatus of claim 26 further comprising an interface module that is structured and arranged to receive a query to display the instrumentation data relating to the ~~design element~~ tri-state bus, wherein the display module is structured and arranged to display the instrumentation data relating to the ~~logic design element~~ tri-state bus in response to the query.

28. (Canceled).

29. (Currently Amended) The apparatus of claim 25 ~~wherein:~~

~~the logic design element includes a tri-state bus, and~~

the collection module is integrated with the tri-state bus and is structured and arranged to automatically collect the instrumentation data relating to the tri-state bus during the simulation.

30-31. (Canceled).

32. (Currently Amended) The ~~machine accessible medium of claim 13~~ method of claim 1 wherein

~~the logic design element represents a FIFO memory, and~~

the instrumentation data collected by the ~~logic design element~~ FIFO memory comprises statistics regarding usage of the FIFO memory.

33. (Currently Amended) The ~~machine accessible medium of claim 13~~ method of claim 1 wherein

~~the logic design element represents a FIFO memory, and~~

the instrumentation data collected by the ~~logic design element~~ FIFO memory comprises a percentage of time a word of the FIFO memory was in use.

34. (Currently Amended) The machine accessible medium of claim 13 wherein

~~the logic design element represents a tri-state bus, and~~

the instrumentation data collected by the ~~logic design element~~ tri-state bus comprises a number of simulation cycles a tri-state bus driver drove the tri-state bus.

35. (Currently Amended) The ~~apparatus of claim 25~~ method of claim 1 wherein

~~the logic design element represents a FIFO memory, and~~

the instrumentation data collected by the collection module of the ~~logic design element~~ FIFO memory comprises a quantity of valid entries present in the FIFO memory during the simulation.

36. (Currently Amended) The ~~apparatus of claim 25~~ method of claim 1 wherein

~~the logic design element represents a FIFO memory, and~~

the instrumentation data collected by the collection module of the ~~logic design element~~ FIFO memory comprises a quantity of read and write pointers used by the FIFO memory during the simulation.

37. (Currently Amended) The apparatus of claim 25 wherein

~~the logic design element represents a tri-state bus, and~~

the instrumentation data collected by the collection module of the ~~logic design element~~ tri-state bus comprises a percentage of time a tri-state bus driver drove the tri-state bus during the simulation.